Add: 2nd Floor, Building C, Jia Huang Yuan Technical Park, Tiegang, Xixiang, Bao'an District, Shenzhen city, Guangdong province, P.R.China 518126.
E-mail: Helen@kingtechgroup.cn TEL: 86-755- 23037763 Mobile: +86-139-2528-0716 Web: www.kingtechgroup.cn

SPECIFICATION FOR LCD Module PV04800TS24A

MODULE:	PV04800TS24A
CUSTOMER:	

KINGTECH	INITIAL	DATE
PREPARED BY	凌传谦	**2015-1-2**
CHECKED BY	尹小军	**2015-1-2**
APPROVED BY	罗教平	**2015-1-2**

CUSTOMER	INITIAL	DATE
APPROVED BY		

Add: 2nd Floor, Building C, Jia Huang Yuan Technical Park, Tiegang, Xixiang, Bao'an District, Shenzhen city, Guangdong province, P.R.China 518126.
E-mail: Helen@kingtechgroup.cn TEL: 86-755- 23037763 Mobile: +86-139-2528-0716 Web: www.kingtechgroup.cn

REVISION STATUS

Version	Revise Date	Page	Content	Modified by
V1.0	2015-1-2	-	First Issued.	Ling
		-		
		-		

Add: 2nd Floor, Building C, Jia Huang Yuan Technical Park, Tiegang, Xixiang, Bao'an District, Shenzhen city, Guangdong province, P.R.China 518126.
E-mail: Helen@kingtechgroup.cn TEL: 86-755- 23037763 Mobile: +86-139-2528-0716 Web: www.kingtechgroup.cn

TABLE OF CONTENTS

1. General Description

*** DESCRIPTION**

PV04800TS24Aisacoloractivematrix TFT(ThinFilmTransistor)LCD(liquidcrystaldisplay) that uses amorphous silicon TFT as a switching device. This model is composed of a Transmissive type TFT-LCD Panel, driver circuit, back-light unit. The resolution of a 4.8" TFT-LCD contains 480 x 1120 pixels, and can display up to 16.7M colors.

*** Features**

-Low Input Voltage: VCI: 2.5~3.3V; IOVCC: 1.65~3.3V
-Display Colors of TFT LCD: 16.7M colors
-CPU Interface: Mipi-2CH
-Internal Power Supply Circuit.

General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	47.95 (H) *112.56(V) (4.8 inch)	mm	-
Driver element	IPS active matrix	-	-
Display colors	16.7M	colors	-
Number of pixels	480(RGB) *1120	dots	-
Pixel arrangement	RGB tilt stripe	-	-
Pixel pitch	0.100(H) *0.132(V)	mm	-
Viewing angle	Free Viewing	o'clock	-
Drive IC	HX8389C	-	-
Display mode	Normally Black	-	-
Operating temperature	-10～+50	℃	-
Storage temperature	-40～+60	℃	-

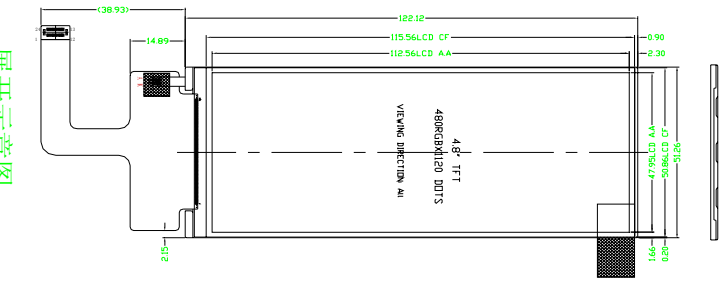
Mechanical Information

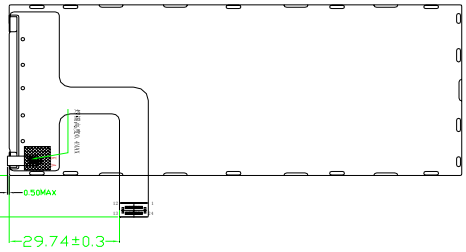
Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)	-	51.26	-	mm	-
	Vertical(V)	-	122.12	-	mm	-
	Depth(D)	-	1.90	-	mm	-
Weight		-	TBD	-	g	-

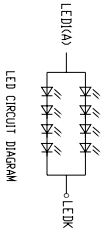
2. MECHANICAL SPECIFICATION

1、Display type:TFT/Normal Black
2、Display mode:Transmissive
3、Interface: 2通道MIPI VIDEO / Driver IC:HX8389C
4、The best Viewing direction: All
5、Backlight: White LED(8-LED) / V=11.6~13.2/ I=40mA
6、LCM Luminance: 280cd/m TYP
7、Operating temprature: -10° C ~ +50° C
8、Storage temprature: -40° C ~ +60° C
9.泡棉视窗单边小于LCD TFT 0.5mm
10、FPC CONNECTOR:AXE624124
11、ROHS REQUEST

展开示意图
弯折出货







LED CIRCUIT DIAGRAM

PIN Definition	SYMBOL
1	NC
2	IC_ID_0
3	RST
4	GND
5	NC
6	NC
7	GND
8	DSI_D1P
9	DSI_D1N
10	GND
11	DSI_CP
12	DSI_CN
13	GND
14	DSI_D0P
15	DSI_D0N
16	GND
17	NC
18	GND
19	TE
20	VDD
21	IOVDD
22	LEDA
23	LEDK
24	LED_PWM

Rev.	Revision content description	Date
A	FIRST ISSUE	2014.06.12
B	EXCHANGED FPC AND CONNECTER	2014.12.16

Kingtech Group Co.,Ltd

TOLERANCE(公差)	Mod.Name	PART.Name
TOLERANCE UNLESS ±0.2	PV04800TS24A	
UNIT: mm	DESIGNED(structure)	DESIGNED(electron)	APPROVED	DRAWING NAME: LCM

SCALE: FIT SHEET: 1/1

3. PIN DESCRIPTION

Pin NO.	Symbol	Level	Function
1	NC		Not Connect
2	IC_ID_0	L	LCM identification PIN
3	RESET	H/L	Global Reset Signal. Active
4	GND	L	Ground
5	NC		Not Connect
6	NC		Not Connect
7	GND	L	Ground
8	DSI_D1P	H/L	MIPI-DSI data Lane 1 positive-end input pin
9	DSI_D1N	H/L	MIPI-DSI data Lane 1 negative-end input pin
10	GND	L	Ground
11	DSI_CP	H/L	MIPI-DSI clock Lane positive-end input pin
12	DSI_CN	H/L	MIPI-DSI clock Lane negative-end input pin
13	GND	L	Not Connect
14	DSI_D0P	H/L	MIPI-DSI data Lane 0 negative-end input pin
15	DSI_D0N	H/L	MIPI-DSI data Lane 0 positive-end input pin
16	GND	L	Ground
17	NC		Not Connect
18	GND	L	Ground
19	TE	H/L	Tearing effect output pin to synchronize MCU to frame writing, activated by S/W command.
20	VDD	H	Power supply to the internal logic power regulator circuit
21	IOVDD	H	A supply voltage to the digital circuit 1.8/2.8V
22	LEDA	H	Backlight+
23	LEDK	H	Backlight-
24	LED_PWM	H/L	LED Pulse-Width Modulation

4. ELECTRICAL CHARACTERISTICS

4.1 ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Values		Unit	Remark
		Min	Max.		
Supply Voltage for Logic circuit	IVOCC	-0.3	+4.4	V	
Supply Voltage for analog circuit	VCI	-0.3	+6.0	V	

4.2 DC ELECTRICAL CHARACTERISTICS

4.2.1 OPERATING CONDITIONS

Typical Operating Conditions (Ta=25℃)

Item	Symbol	Values			Unit	Remark
		Min	Typ	Max.		
Power Supply	VCI	2.3	2.8	5.5	V	
Normal mode Current consumption	Icc	-	45	-	mA	V_{CI}=2.8V
TFT Gate ON Voltage	V_{GH}	-0.3	-	25	V	
TFT Gate OFF Voltage	V_{GL}	-18	-	0	V	

4.2.2 BACKLIGHT UNIT (GND=0V)

Item	Symbol	Values			Unit	Remark
		Min	Typ	Max.		
Forward supply Voltage	V_f	11.6		13..2	V	
Forward supply Current	I_f	-	40	-	mA	
LCM Luminance	LV		280	-	cd/m2	IB=40mA
BL Luminance	LV	7000			cd/m2	IB=40mA
LED backlight lifetime for LCM	/			50000	H	
Uniformity	/	80			%	-

4.3 TIMING CHARACTERISTICS

4.3.1 The Electrical Characteristics of D-PHY Layer

In general, the DSI D-PHY may contain the following electrical functions: High-Speed Receiver (HS-RX), Low Power Transmitter (LP-TX), a Low-Power Receiver (LP-RX), and the Low-Power Contention Detector (LP-CD). Figure 7.6 shows the complete set of electrical functions required for a fully featured PHY transceiver.

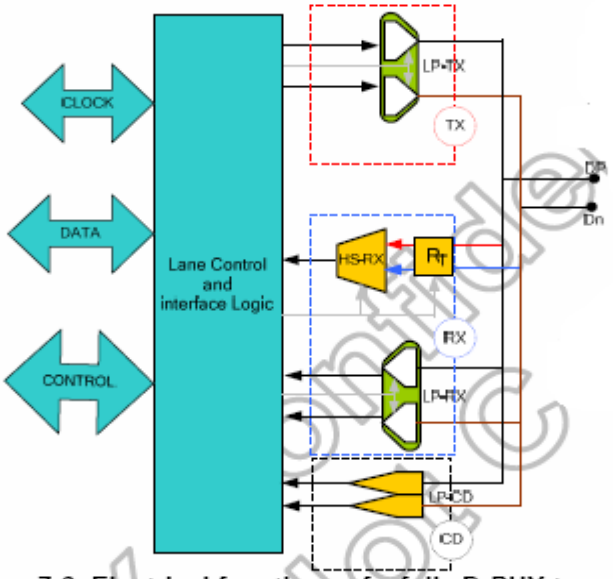


Figure 7.6: Electrical functions of a fully D-PHY transceiver

Where, the HS receiver utilize low-voltage swing differential signaling for signal transmission. The LP transmitter and LP receiver serve as a low power signaling mechanism. The Figure 8.7 shows both the HS and LP signal levels on the left and right sides, respectively.

Because the HS signaling levels are below the LP low-level input threshold, Lane switches between Low-Power and High-Speed mode during normal operation.

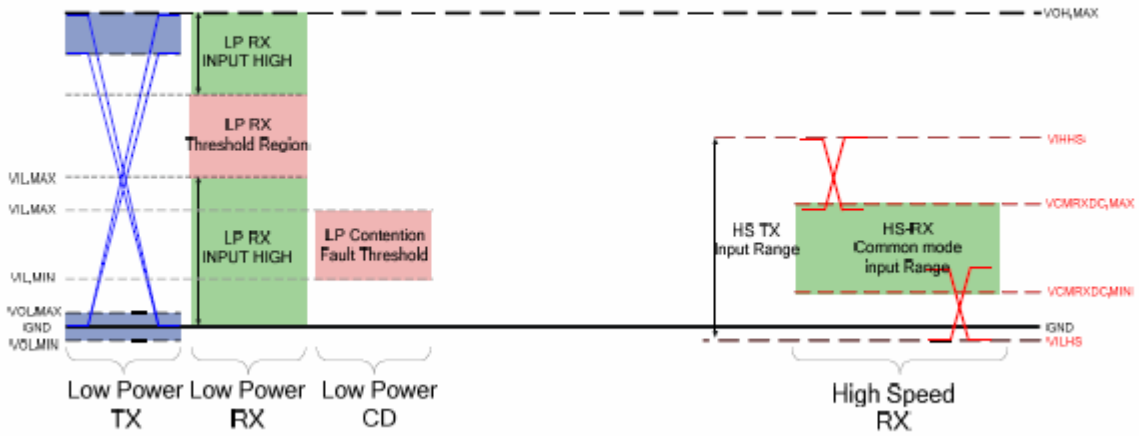


Figure 7.7: Shows both the HS and LP signal levels

4.3.2 The Electrical Characteristics of Low-Power Transmitter

The Low-Power transmitter shall be a slew-rate controlled push-pull driver. It is used for driving the Lines in all Low-Power operating modes It is therefore important that the static power consumption of a LP transmitter be as low as possible. Under tables list DC and AC characteristic for LP-TX

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{OL}	Thevenin output low level	-50	-	50	mV	-
V_{OH}	Thevenin output high level	1.1	1.2	1.3	V	-
Z_{OLP}	Output impedance of LP-TX	110	-	-	Ω	(1)

Note: (1)Though no maximum value for Z_{OLP} is specified, the LP transmitter output impedance shall ensure the t_{RLP}/t_{FLP} specification is met.

Table 7.8: LP Transmitter DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
t_{RLP}/t_{FLP}	15%-85% rise time and fall time	-	-	25	ns	(1)
T_{LPX}	Transmitted length of any Low-Power state period	50	-	-	ns	TX_OSC=0 (10)
		100	-	-	ns	TX_OSC=1 (10)
$\delta V/\delta t_{SR}$	Slew rate @ C_{LOAD} = 0pF	-	-	500	mV/ns	(1),(3),(5),(6)
	Slew rate @ C_{LOAD} = 5pF	-	-	300	mV/ns	(1),(3),(5),(6)
	Slew rate @ C_{LOAD} = 20pF	-	-	250	mV/ns	(1),(3),(5),(6)
	Slew rate @ C_{LOAD} = 70pF	-	-	150	mV/ns	(1),(3),(5),(6)
	Slew rate @ C_{LOAD} = 0 to 70pF (Falling Edge Only)	30	-	-	mV/ns	(1),(2),(3)
	Slew rate @ C_{LOAD} = 0 to 70pF (Rising Edge Only)	30	-	-	mV/ns	(1),(3),(7)
	Slew rate @ C_{LOAD} = 0 to 70pF (Rising Edge Only)	30 – 0.075 * (VO,INST- 700)	-	-	mV/ns	(1),(8),(9)
C_{LOAD}	Load capacitance	0	-	70	pF	-

Note: (1) C_{LOAD} includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.
(2) When the output voltage is between 400 mV and 930 mV.
(3) Measured as average across any 50 mV segment of the output signal transition.
(4) This parameter value can be lower than TLPX due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters.
(5) This value represents a corner point in a piecewise linear curve.
(6) When the output voltage is in the range specified by VPIN(absmax).
(7) When the output voltage is between 400 mV and 700 mV.
(8) Where VO,INST is the instantaneous output voltage, VDP or VDN, in millivolts.
(9) When the output voltage is between 700 mV and 930 mV.
(10) TX_OSC is internal register setting.

4.3.3 The Electrical Characteristics of Receiver

This part will contain two parts which High-Speed Receiver and Low-Power Receiver. Because their have differential DC and AC characteristic, describe HS-RX first then describe LP-RX.

4.3.4High-Speed Receiver

The HS receiver is a differential line receiver. It contains a switch-able parallel input termination, Z_{ID}, between the positive input pin Dp and the negative input pin Dn. Under Tables list DC and AC characteristic for HS-RX.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{IDTH}	Differential input high threshold	-	-	70	mV	-
V_{IDTL}	Differential input low threshold	-70	-	-	mV	-
V_{ILHS}	Single-ended input low voltage	-40	-	-	mV	(1)
V_{IHHS}	Single-ended input high voltage	-	-	460	mV	(1)
V_{CMRXDC}	Common-mode voltage HS receive mode	70	-	330	mV	(1),(2)
Z_{ID}	Differential input impedance	80	100	125	Ω	-

Note: (1) Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.
(2) This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz

Table 7.10: HS Receiver DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
$\Delta V_{CMRX(HF)}$	Common mode interference beyond 450 MHz	-	-	100	mV_{PP}	(1)
C_{CM}	Common mode termination	-	-	60	pF	(2)

Note: (1) $\Delta V_{CMRX(HF)}$ is the peak amplitude of a sine wave superimposed on the receiver inputs.
(2) For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

Table 7.11: HS Receiver AC Specifications

4.3.5 Low-Power Receiver

The low power receiver is an un-terminated, single-ended receiver circuit. The LP receiver is used to detect the Low-Power state on each pin. For high robustness, the LP receiver shall filter out noise pulses and RF interference. It is recommended the implementer optimize the LP receiver design for low power. The LP receiver shall reject any input glitch when the glitch is smaller than eSpike. The filter shall allow pulses wider than TMIN to propagate through the LP receiver. The related diagram shows as Figure 7.8 Input Glitch Rejection of Low-Power Receivers. Besides, under tables list DC and AC characteristic for LP-RX.

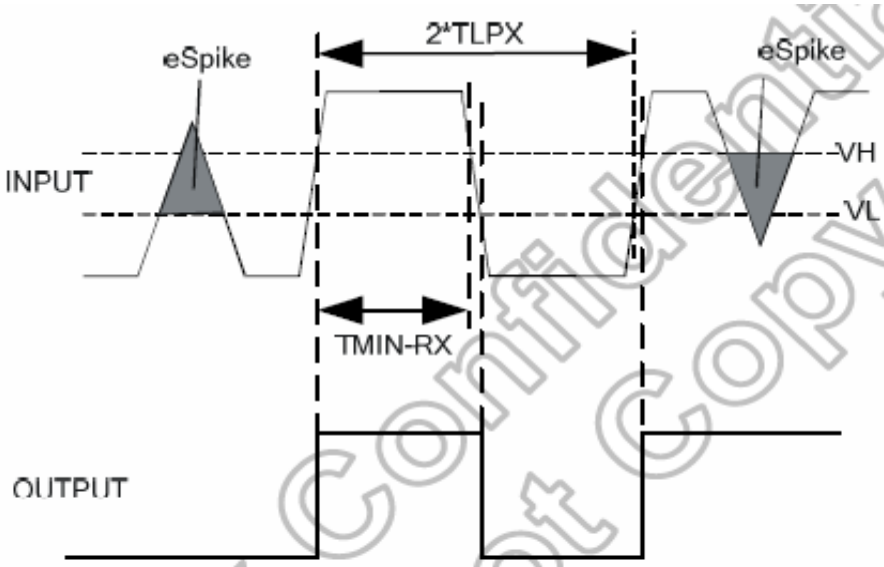


Figure 7.8: Input Glitch Rejections of Low-Power Receivers

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{IL}	Logic 0 input threshold	-	-	550	mV	-
V_{IH}	Logic 1 input threshold	880	-	-	mV	-

Table 7.12: LP Receiver DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
e_{SPIKE}	Input pulse rejection	-	-	300	V.ps	1, 2, 3
T_{MIN-RX}	Minimum pulse width response	20	-	-	ns	4
V_{INT}	Peak-to-peak interference voltage	-	-	200	mV	-
f_{INT}	Interference frequency	450	-	-	MHz	-

Note: (1) Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1 state
(2) An impulse less than this will not change the receiver state.
(3) In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.
(4) An input pulse greater than this shall toggle the output.

4.5.6 High-Speed Data-Clock Timing

This section specifies the required timings on the high-speed signaling interface independent of the electrical characteristics of the signal. The PHY is a source synchronous interface in the Forward direction.

The Master side of the Link shall send a differential clock signal to the Slave side to be used for data sampling. This signal shall be a DDR (half-rate) clock and shall have one transition per data bit time. All timing relationships required for correct data sampling are defined relative to the clock transitions. Therefore, implementations may use frequency spreading modulation on the clock to reduce EMI.

The DDR clock signal shall maintain a quadrature phase relationship to the data signal. Data shall be sampled on both the rising and falling edges of the Clock signal. The term "rising edge" means "rising edge of the differential signal, i.e. CP – CN, and similarly for "falling edge". Therefore, the period of the Clock signal shall be the sum of two successive instantaneous data bit times. This relationship is shown in Figure 7.9.

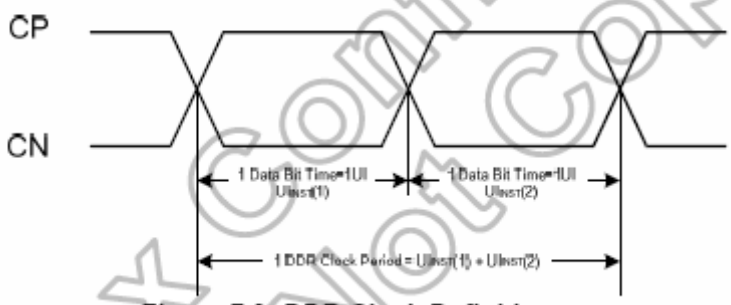


Figure 7.9: DDR Clock Definition

The same clock source is used to generate the DDR Clock and launch the serial data. Since the Clock and Data signals propagate together over a channel of specified skew, the Clock may be used directly to sample the Data lines in the receiver. Such a system can accommodate large instantaneous variations in UI.

The allowed instantaneous UI variation can cause large, instantaneous data rate variations. Therefore, devices shall either accommodate these instantaneous variations with appropriate FIFO logic outside of the PHY or provide an accurate clock source to the Lane Module to eliminate these instantaneous variations.

The UI_{INST} specifications for the Clock signal are summarized in Table 7.15.

DSI Mode	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
650Mbps @ 2-lane	UI instantaneous	UI_{INST}	1.54	-	12.5	ns	(1)
500Mbps @ 3-lane			2	-	12.5	ns	(2)

Note: (1) This value 1.54ns corresponds to a maximum 650 Mbps data rate, 12.5ns corresponds to a minimum 80 Mbps data rate
(2) This value 2ns corresponds to a maximum 500 Mbps data rate, 12.5ns corresponds to a minimum 80 Mbps data rate

Table 7.15: Reverse HS Data Transmission Timing Parameters

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 7.10. Data is launched in a quadrature relationship to the clock such that the Clock signal edge may be used directly by the receiver to sample the received data.

The transmitter shall ensure that a rising edge of the DDR clock is sent during the first payload bit of a transmission burst such that the first payload bit can be sampled by the receiver on the rising clock edge, the second bit can be sampled on the falling edge, and all following bits can be sampled on alternating rising and falling edges.

All timing values are measured with respect to the actual observed crossing of the Clock differential signal. The effects due to variations in this level are included in the clock to data timing budget.

Receiver input offset and threshold effects shall be accounted as part of the receiver setup and hold parameters.

Receiver input offset and threshold effects shall be accounted as part of the receiver setup and hold parameters.

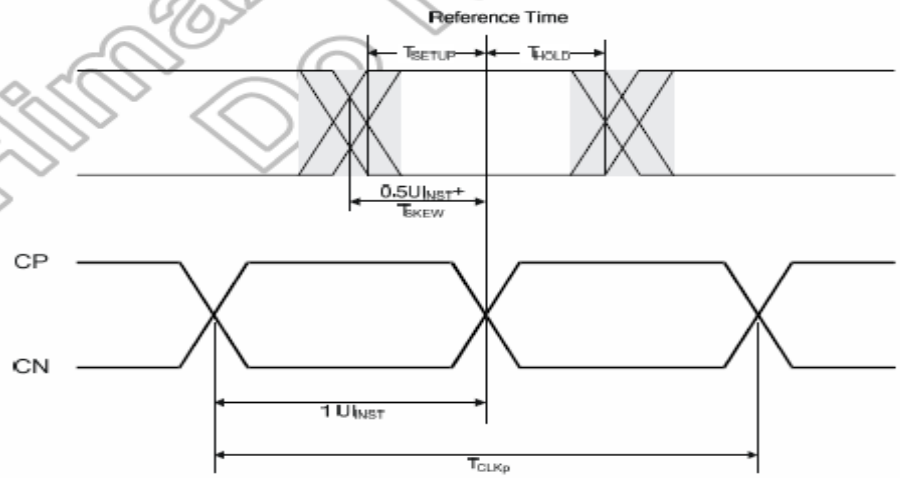


Figure 7.10: Data to Clock Timing Definitions

5.0 Optical Characteristics

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Threshold Voltage		Vsat		4.1	4.3	4.5	V	Fig.1
		Vth		1.6	1.8	2.0	V	
Viewing Angle	Horizontal	Θ3	CR>10	70	80		°	Note 1
		Θ9		70	80		°	
	Vertical	Θ12		70	80		°	
		Θ6		70	80		°	
Contrast Ratio		CR	Θ= 0°		900			Note 2
Transmittance		T(%)	Θ= 0°		3.7			Note 3
NTSC		%	Θ= 0°		70			
Reproduction Of color	Red	Rx	Θ= 0°	0.641	0.656	0.671		Note 4 *Color filter Glass with OC
		Ry		0.312	0.327	0.342		
	Green	Gx		0.273	0.288	0.303		
		Gy		0.575	0.590	0.605		
	Blue	Bx		0.123	0.138	0.153		
		By		0.096	0.111	0.126		
White		Wx	Θ= 0°	0.287	0.302	0.317		
		Wy		0.314	0.329	0.344		
Response Time		Tr+Tf	Θ= 0°		25		ms	Note 5

Note:

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see FIG.2).
2. Contrast measurements shall be made at viewing angle of Θ= 0° and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (See FIG. 2) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Transmittance is the value with APF Pol.

4. The color chromaticity coordinates specified in Table1 shall be calculated from
The spectral data measured with all pixels first in red, green, blue and white.
Measurements shall be made at the center of the C/F.
Measurement condition is C - light source & Halogen Lamp
5. The electro-optical response time measurements shall be made as FIG.3 by switching the "data" input signal ON and OFF.

The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Tf.

Figure 1. The definition of Vth & Vsat

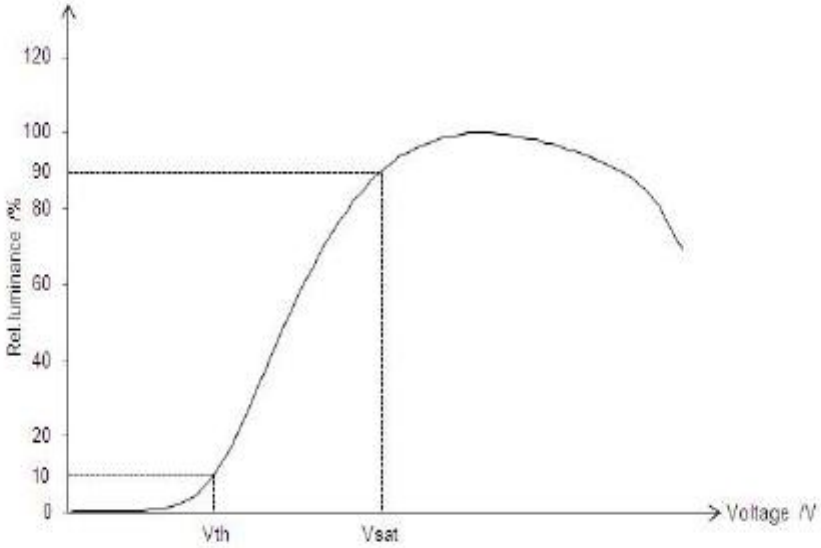


Figure 2. Measurement Set Up

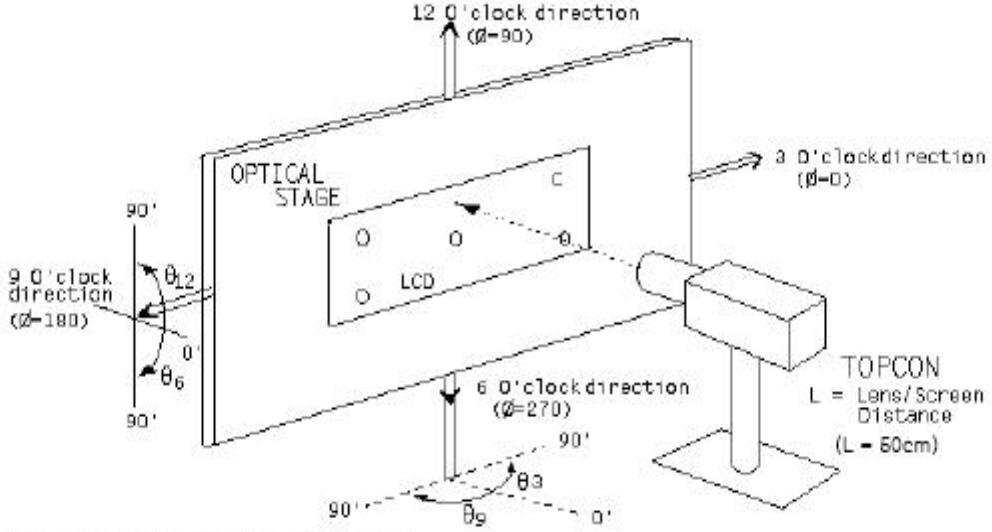
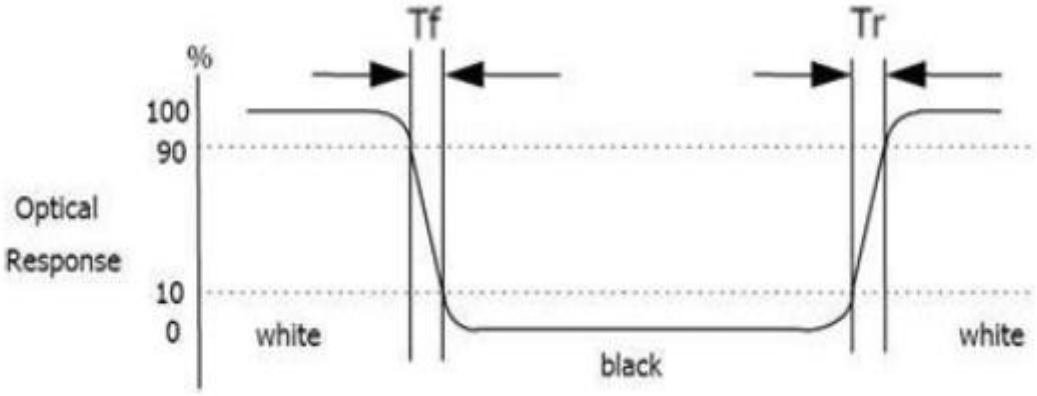


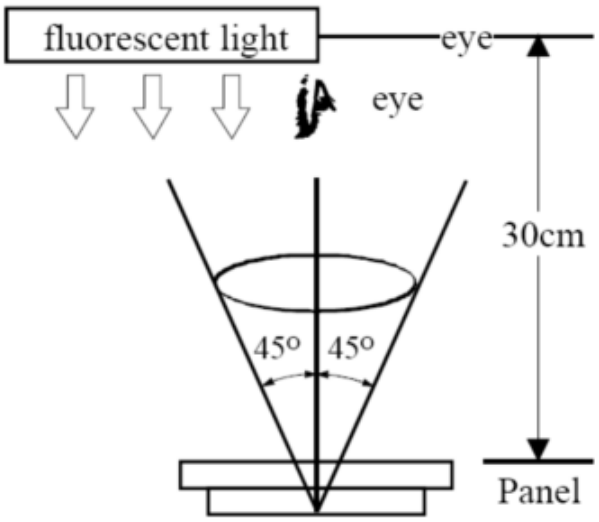
Figure 3. Response Time Testing



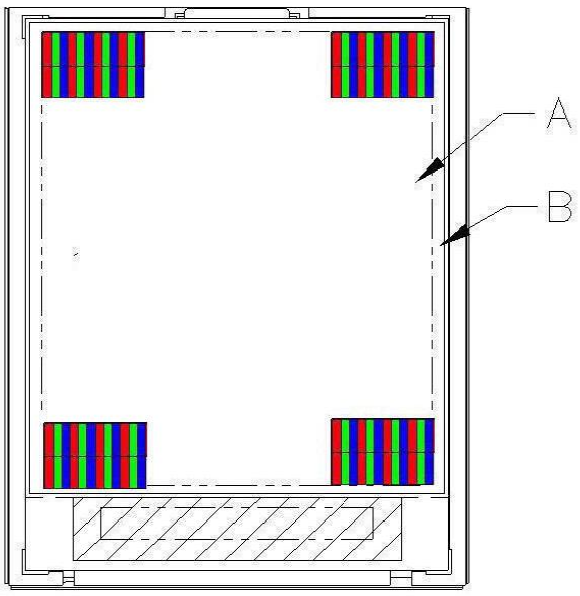
6. QUALITY SPECIFICATIONS

6.1 INSPECTION CONDITION

(1) Inspect under 300~500Lux fluorescent light, leaving 30~35cm between panels and eyes, and between panels and lights.
(2) Inspection condition is 23±5°C, 50±20%RH maximum.

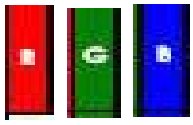
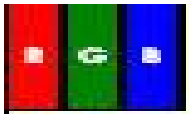


6.2 DEFINITION OF AREA



A Area : Viewing area.
B Area : Out of viewing.(outside viewing area)

6.3 INSPECTION SPECIFICATION

NO	Item	Acceptable specification	Judgment Criterion
1	Electrical Testing	**1-1 sub pixel classification** ● Sub Pixel: Number of sub pixel doesn't exceed one dot.  **Sub Pixel (Dot)** **a> Dark dot ----one Allowed** **b> Bright dot ---- one Allowed**	N≦1
		● Pixel : Three dots link together doesn't exceed ones  **Pixel**	N≦0
		1-2 Leakage to light ● Leakage to light be not allowed.	N=0
		1-3 Picture to shake ● Picture had shake, twinkle and noise etc. instable of defect that be not allowed.	N=0
		1-4 Function ● No display or No function. ● Source Line, Gate Line. ● Contrast Ratio ● Current consumption exceeds product specifications. ● Display malfunction.	N=0
2	Mechanical Dimension	2-1 Mechanical Dimension exceeds product specifications. 2-2 Out of frame and boss of plastic changed shape that be not allowed.	N=0

<table>
<tr><th>NO</th><th>Item</th><th>Acceptable specification</th><th>Judgment Criterion</th></tr>
<tr><td>3</td><td>Cosmetic Inspection</td><td>

3-1 Blemish: Line shapes of defect

<table>
<tr><th>Length</th><th>Width</th><th>Acceptable number</th><th>Mini. space</th></tr>
<tr><td>---</td><td>W≦0.03</td><td>Ignore</td><td rowspan="3">5 m m</td></tr>
<tr><td>L≦2.5</td><td>0.03<W≦0.05</td><td>3</td></tr>
<tr><td>L≦2.5</td><td>0.05<W≦0.1</td><td>2</td></tr>
<tr><td>--</td><td>W＞0.1</td><td>Not allowed</td><td>---</td></tr>
</table>

L: length(mm)
W: width(mm)

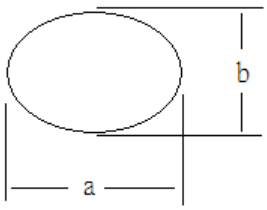
3-2 Blemish: dot shapes of defect.

<table>
<tr><th>Dimension</th><th>Acceptable number</th><th>Mini. Space</th></tr>
<tr><td>Φ≦0.10</td><td>Ignore</td><td>---</td></tr>
<tr><td>0.10＜Φ≦0.15</td><td>2</td><td rowspan="2">5 m m</td></tr>
<tr><td>0.15＜Φ≦0.25</td><td>1</td></tr>
<tr><td>Φ＞0.25</td><td>0</td><td>---</td></tr>
</table>

3-3 Polarizer Bubble

<table>
<tr><th>Dimension</th><th>Acceptable number</th><th>Mini. Space</th></tr>
<tr><td>Φ≦0.20</td><td>Ignore</td><td>---</td></tr>
<tr><td>0.20＜Φ≦0.30</td><td>2</td><td>15 m m</td></tr>
<tr><td>Φ＞0.30</td><td>0</td><td>---</td></tr>
</table>

Foreign Substances



Φ=(a+b)/2

</td><td></td></tr>
</table>

Add: 2nd Floor, Building C, Jia Huang Yuan Technical Park, Tiegang, Xixiang, Bao'an District, Shenzhen city, Guangdong province, P.R.China 518126.
E-mail: Helen@kingtechgroup.cn TEL: 86-755- 23037763 Mobile: +86-139-2528-0716 Web: www.kingtechgroup.cn

<table>
<tr><th>NO</th><th>Item</th><th>Acceptable specification</th><th>Judgment Criterion</th></tr>
<tr><td>3</td><td>Cosmetic Inspection</td><td>
3-4 Scratch
● Sensate scratch not allowed.
● Impassive scratch as below.
Unit:mm
<table>
<tr><th>Length</th><th>Width</th><th>Acceptable number</th><th>Mini. space</th></tr>
<tr><td>-----</td><td>W≦0.03</td><td>Ignore</td><td rowspan="3">5 m m</td></tr>
<tr><td>L≦2.5</td><td>0.03<W≦0.05</td><td>3</td></tr>
<tr><td>L≦2.5</td><td>0.05<W≦0.1</td><td>2</td></tr>
<tr><td>----</td><td>0.1＜W</td><td>Not allowed</td><td rowspan="2">---</td></tr>
<tr><td>L>2.5</td><td>----</td><td>Not allowed</td></tr>
</table>
</td><td></td></tr>
<tr><td>4</td><td>Package</td><td>4-1 Mixed product types
4-2 Shipping q'ty should be the same as "shipping notice form" q'ty.
4-3 Outer box can't broken.</td><td>N=0</td></tr>
</table>

7. RELIABILITY

Test Item	Test Condition
High Temperature Operation	50℃ for 96 hours
Low Temperature Operation	-10℃ for 96 hours
High Temperature Storage	60℃ for 96 hours
Low Temperature Storage	-40℃ for 96 hours
High Temperature Operation Humidity Operation	50℃, 95%RH for 96 hours
Thermal Shock	-10℃(30min) ~+25℃(5min)~ +50℃(30min) for 10 cycles
Vibration Test (No Operation)	Frequency: 10~55Hz Amplitude:1.0mm Sweep Time: 11min Test Period: 6 Cycles for each direction of X, Y, Z

Add: 2nd Floor, Building C, Jia Huang Yuan Technical Park, Tiegang, Xixiang, Bao'an District, Shenzhen city, Guangdong province, P.R.China 518126.
E-mail: Helen@kingtechgroup.cn TEL: 86-755- 23037763 Mobile: +86-139-2528-0716 Web: www.kingtechgroup.cn

8. HANDLING PRECAUTION

8.1 SAFETY

(1) Do not swallow any liquid crystal, even if there is no proof that liquid stal is poisonous.
(2) If the LCD panel breaks, be careful not to get liquid crystal to touch your skin.
(3) If skin is exposed to liquid crystal, wash the area thoroughly with alcohol or soap.

8.2 STORAGE CONDITIONS

(1) Store the panel or module in a dark place where the temperature is 23±5℃ and thehumidity is below 50±20%RH.
(2) Store in anti-static electricity container.
(3) Store in clean environment, free from dust, active gas, and solvent.
(4) Do not place the module near organics solvents or corrosive gases.
(5) Do not crush, shake, or jolt the module.

8.3 HANDLING PRECAUTIONS

(1) Avoid static electricity which can damage the CMOS LSI.
(2) The polarizing plate of the display is very fragile. So, please handle it very carefully.
(3) Do not give external shock.
(4) Do not apply excessive force on the surface.
(5) Do not wipe the polarizing plate with a dry cloth, as it may easily scratch the surface of plate.
(6) Do not use ketonics solvent & Aromatic solvent, use with a soft cloth soaked with acleaning naphtha solvent.
(7) Do not operate it above the absolute maximum rating.
(8) Do not remove the panel or frame from the module.

8.4 WARRANTY

The period is within twelve months since the date of shipping out under normal using and storage conditions.